

**Notice of Allowability**

Application No.

10/071,647

Examiner

Michael S. Lebentritt

Applicant(s)

PARK ET AL.

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment 1/30/04.
2. ☒ The allowed claim(s) is/are 1-12 and 59-104.
3. ☒ The drawings filed on 08 February 2002 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☒ Certified copies of the priority documents have been received in Application No. 09/105,732.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.


**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

  
Michael S. Lebentritt  
Primary Examiner  
Art Unit: 2824

### **REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance: the priors art references fail to either singularly or in combination teach:

depositing a passivation layer over the first surface of the substrate; patterning the passivation layer to form a first contact hole exposing a portion of the drain electrode; depositing a transparent conductive layer; coating a negative photoresist on the transparent conductive layer; and exposing the negative photoresist by irradiating light from the first surface of the substrate using a first mask having first openings at positions corresponding to the first contact hole and the pixel region; developing the negative photoresist; and etching the transparent conductive layer by using the negative photoresist as an etch mask to form a pixel electrode connected to the drain electrode via the first contact hole as specified in claim 1. Further: patterning the passivation layer to form a first contact hole exposing a portion of the drain electrode; depositing a transparent conductive layer; coating a negative photoresist on the transparent conductive layer; rear exposing the negative photoresist by irradiating light from the second surface of the substrate, front exposing the negative photoresist by irradiating light from the first surface of the substrate and using a first mask having a first opening at positions corresponding to the first contact hole; developing the negative photoresist; and etching the transparent conductive layer by using the negative photoresist as a etch mask to form a pixel electrode connected to the drain electrode via the first contact hole as specified in claim 6. Also: a plurality of thin film transistors each having a drain electrode and a source electrode electrically connected to the data line; a passivation

Art Unit: 2824

layer covering the gate wire, the data wire and the thin film transistors and having first, second and third contact holes which expose the gate pad, the data pad and the drain electrode at least in part respectively; a pixel electrode on the passivation film, the pixel electrode connected to the drain electrode through the third contact hole and overlapping at least a part of the data lines adjacent to the pixel electrode; a first conductor on the passivation film, the first conductor connected to the gate pad through the first contact hole; and a second conductor on the passivation film, the second conductor connected to the data pad through the second contact hole as specified in claim 59. Also further: a plurality of thin film transistors, each having a drain electrode and a source electrode electrically connected to the data line; a passivation layer covering the gate lines, the data lines and the thin film transistors, the passivation layer having a first contact hole which expose the drain electrode at least in part; a pixel electrode on the passivation film, the pixel electrode connected to the drain electrode through the first contact hole, overlapping a part of the data lines adjacent to the pixel electrode; and a first conductor including a layer different from the pixel electrode, electrically connected to the pixel electrode and serving as a terminal of a storage capacitor as specified in claim 76. Further: a data line on the insulating substrate; a thin film transistor on the insulating substrate wherein the thin film transistor comprises a pair of source/drains wherein a first of the pair of source/drains is coupled to the data line; a passivation layer on the gate line, on the data line, and on the thin film transistor so that the gate line, the data line, and the thin film transistor are between the insulating substrate and the passivation layer wherein the passivation layer has a contact hole

Art Unit: 2824

therein exposing a portion of a second of the pair of source/drains of the thin film transistor; and a pixel electrode on the passivation layer so that the passivation layer is between the pixel electrode and the insulating substrate wherein the pixel electrode is coupled with the second of the pair of source/drains of the thin film transistor through the contact hole in the passivation layer and wherein the pixel electrode extends onto a portion of the data line so that the portion of the data line is between the pixel electrode extending thereon and the insulating substrate as specified in claim 89.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael S. Lebentritt whose telephone number is 571-272-1873. The examiner can normally be reached on 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2824

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Michael S. Lebentritt  
Primary Examiner  
Art Unit 2824

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